CLAIMS

We claim:

1   1.   A method comprising:

2   commencing execution of a first set of one or more write instructions,

3   wherein the write instructions of the first set are the width of a

4   processor data bus;

5   aborting the execution of the first set of write instructions;

6   creating a second set of one or more write instructions, in response to the

7   aborting, wherein the write instructions of the second set are the

8   width of an expansion bus; and

9   executing the second set of write instructions.

1   2.   The method of claim 1, wherein the width of the processor bus is 32 bits.

1   3.   The method of claim 1, wherein the width of the expansion bus is 16 bits.

1   4.   The method of claim 1, wherein the second set of write instructions are

2   suitable for transmission over the expansion bus.

1   5.   A method comprising:

2   executing a write instruction that writes to a virtual memory address;

3   translating the virtual memory address, wherein translating includes

4   determining whether the virtual memory address maps to an

5   inaccessible physical memory address;

6   generating an abort indication after determining that the virtual memory

7   address maps to an inaccessible physical memory address;

8   performing the following in response to the abort indication,

9   creating multiple write instructions suited for transmission over an

10   expansion bus; and

11   executing the multiple write instructions.

1   6.   The method of claim 5, wherein the expansion bus is 16 bits wide.

1   7.   The method of claim 6, wherein the write instruction is a 32-bit write
2   instruction.

1   8.   The method of claim 6, wherein the write instruction is wider than the
2   expansion bus.

1   9.   An apparatus comprising:
2   a memory management unit to receive a virtual address, the memory
3   management unit to determine whether the virtual address maps to an
4   inaccessible physical address and to transmit an abort indication if
5   the virtual address maps to an inaccessible address; and

6   a processor core to receive the abort indication from the memory management unit
7   and to execute instructions, the processor core including an abort handler to create
8   new instructions in response to receipt of the abort indication, wherein the new
9   instructions are the width of an expansion bus.

1   10.   The apparatus of claim 9, wherein a physical address is inaccessible if it is
2   write-protected.

1   11.   The apparatus of claim 9 further comprising:

2   an external expansion device communicatively coupled to the processor core, the
3   external expansion device to receive the new instructions over the expansion bus.

1   12.   The apparatus of claim 11, wherein the expansion bus is 16 bits wide.

1   13.   The apparatus of claim 9, wherein instructions are 32-bit instructions.

1   14.   A system comprising:
2   a processor, the processor including,

3   a processor core to receive an abort indication, wherein the processor

4   core includes an abort handler to create new write instructions

5   suited for transmission over an expansion bus; and

6   a memory management unit (MMU) coupled to the processor core by

7   a processor data bus, the MMU to determine whether a virtual

8   memory address maps to an accessible physical memory

9   address, the MMU to transmit the abort indication to the

10   processor core if the virtual memory address does not map to

11   an accessible physical memory address;

12   an external expansion device to receive the new write instructions from the

13   processor over the expansion bus; and

14   a dynamic random access memory (DRAM) unit coupled to the processor, wherein

15   the DRAM unit is to store data accessible by the processor.

1   15.   The system of claim 14, wherein the expansion bus is half the width of the

2   processor data bus.

1   16.   The system of claim 14, wherein the abort indication includes the virtual

2   memory address.

1   17.   The system of claim 14, wherein the external expansion device is a flash

2   memory device.

1   18.   A machine-readable medium that provides instructions, which when

2   executed by a machine, cause the machine to perform operations comprising:

3   commencing execution of a first set of one or more write instructions,

4   wherein the write instructions of the first set are the width of a

5   processor data bus;

6   aborting the execution of the first set of write instructions;

7   in response to the aborting, creating a second set of one or more write

8   instructions, wherein the write instructions of the second set are the

9   width of an expansion bus;

10   executing the second set of write instructions.

1   19.   The machine-readable medium of claim 18, wherein the width of the

2   processor bus is 32 bits.

1   20.   The machine-readable medium of claim 18, wherein the width of the

2   expansion bus is 16 bits.

1   21.   The machine-readable medium of claim 18, wherein the second set of write

2   instructions are suitable for transmission over the expansion bus.

1   22.   A machine-readable medium that provides instructions, which when

2   executed by a machine, cause the machine to perform operations comprising:

3   executing a write instruction that writes to a virtual memory address;

4   translating the virtual memory address, wherein translating includes

5   determining whether the virtual memory address maps to an

6   inaccessible physical memory address;

7   after determining whether the virtual memory address maps to an

8   inaccessible physical memory address, generating an abort

9   indication;

10   receiving the abort indication, and

11   creating multiple write instructions suited for transmission over an

12   expansion bus; and

13   executing the multiple write instructions.

1   23.   The machine-readable medium of claim 22, wherein the expansion bus is 16

2   bits wide.

1   24.   The machine-readable medium of claim 22, wherein the write instruction is a
2   32-bit instruction.

1   25.   The machine-readable medium of claim 22, wherein the write instruction is
2   wider than the expansion bus.